

Substitute for Form 1449/PTO

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

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Complete if Known

Application Number	09/752,541
Filing Date	12-29-00
First Named Inventor:	Boyd, et al.
Art Unit	2124
Examiner Name	Tuan A. Vu
Attorney Docket Number	004363.P001

Sheet

of

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
MJS ↓ JAT		US-	5,973,524	10/26/1999	Martin	
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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
MJS		GB	2 131 228 A		6/13/1984	RCA Corporation		

Examiner
Signature

Tuan A. Vu

Date Considered

09-09-05

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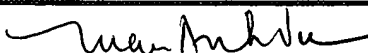
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NON PATENT LITERATURE DOCUMENTS			
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AT		MEDIERO, F., et al., "A Vertically Integrated Tool For Automated Design Of Sigma Delta Modulators", IEEE Journal of Solid-State Circuits, Vol. 30., No. 7, July 1, 1995, pp. 762-767.	
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Examiner Signature		Date Considered	9-9-05
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<div style="border: 1px solid black; border-radius: 50%; width: 100px; height: 100px; display: flex; align-items: center; justify-content: center; margin: 0 auto;"> <div style="text-align: center;"> U.S. PATENT & TRADEMARK OFFICE JUN 27 2005 </div> </div>				Application Number: 09/752,541	
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NON PATENT LITERATURE DOCUMENTS					
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CAT		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.			
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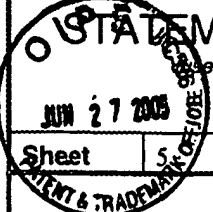
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NAT		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.			
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NAT		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.			

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